Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A method for memory allocation for a multithreaded processor, comprising:

obtaining threads of different types;

~~creating sets from the~~ determining a set of threads ~~according to thread,~~ each of a same type;

~~allocating memory space for each thread in a set responsive to the thread type of the set~~ determining a first contiguous memory section to be allocated to said set of threads; and

~~allocating memory spaces for data buffers accessible by the threads~~ determining a second contiguous memory section to be allocated to a data buffer,

wherein memory spaces in the first contiguous memory section are accessible by the threads in said set of threads and memory spaces in the second contiguous memory section are accessible by any of said threads of different types.

Claim 2 (Currently Amended): The method according to claim 1, wherein a ~~location in a data buffer~~ memory space in the second contiguous memory section is written to by a first thread and read from by ~~another~~ a second thread.

Claim 3 (Original): The method according to claim 1, further comprising:

determining if a read-after-write hazard exists for a location in a memory space for a thread.

Claim 4 (Currently Amended): The method according to claim 1, wherein a position in the data buffer, to which data is to be written or from which data is to be read, is determined by a thread.

Claim 5 (Currently Amended): The method according to claim 1, wherein [[a]] the data buffer is associated with a buffer identifier.

Claim 6 (Original): The method according to claim 5, wherein a memory location address in the data buffer is determined using the buffer identifier and position coordinates associated with a sample.

Claim 7 (Currently Amended): The method according to claim 1, further comprising determining a third contiguous memory section to be allocated to another data buffer, wherein a size of ~~a data buffer is different than a size of another data buffer~~ the second contiguous memory section is different than a size of the third contiguous memory section.

Claim 8 (Currently Amended): A method for accessing a memory resource having memory spaces allocated for a plurality of threads simultaneously executable in a graphics processor ~~responsive to a graphics program module~~, comprising:

~~processing a first sample by a first thread; and~~

~~processing a second sample by a second thread;~~

~~wherein a first memory space is accessed only by the first thread during processing of the first sample by the first thread, a second memory space is accessed only by the second thread during processing of the second sample by the second thread, and a third memory space is accessed by the first thread and the second thread~~

simultaneously processing a first sample by threads of a first type and a second sample by threads of a second type, wherein during the simultaneously processing: (i) a first contiguous memory section allocated to threads of the first type is accessed by threads of the first type, but not by threads of the second type, (ii) a second contiguous memory section allocated to threads of the second type is accessed by threads of the second type, but not by threads of the first type, and (iii) a third contiguous memory section allocated to a data buffer is accessed by threads of either the first type or the second type.

Claim 9 (Currently Amended): The method according to claim 8, wherein the third contiguous memory ~~space~~ section stores data ~~buffers~~ for the data buffer.

Claim 10 (Currently Amended): The method according to claim 8, wherein ~~the first thread~~ a thread of the first type determines a position in [[a]] the data buffer, to which data is to be written or from which data is to be read.

Claim 11 (Original): The method according to claim 8, further comprising:

determining if a read after write hazard exists for a location in a memory space accessed by a thread.

Claim 12 (Currently Amended): The method according to claim 8, further comprising:

writing sample data to a ~~location in a data buffer by the first thread~~ memory space in the third contiguous memory section by a thread of the first type; and

reading the sample data from ~~the location in the data buffer by the second thread~~ said memory space in the third contiguous memory section by a thread of the second type.

Claim 13 (Currently Amended): The method according to claim 8, wherein the data buffer ~~in the third memory space~~ is associated with a buffer identifier.

Claim 14 (Currently Amended): A computer program product having a computer readable medium having computer program instructions recorded thereon, said computer program product comprising:

instructions for determining a ~~first~~ set of threads [[of]] , each of a same type, from a plurality of threads~~, each thread in the plurality of threads being associated with a graphics program module executing~~ executable on a graphics processor;

instructions for allocating ~~a first memory space~~ memory spaces in a first contiguous memory ~~resource~~ section to ~~each thread~~ the threads in ~~the first~~ said set of threads, ~~the first~~ said memory spaces in the first contiguous memory ~~space~~

section being reserved for ~~the thread to which the first memory space is allocated~~ use by the threads in said set of threads; and

instructions for allocating ~~a second memory space~~ memory spaces in [[the]] a second contiguous memory ~~resource~~ section to a data buffer, ~~the data buffer~~ said memory spaces in the second contiguous memory section being accessible by ~~each thread in~~ any one of the plurality of threads.

Claim 15 (Currently Amended): The computer program product of claim 14, wherein a first thread writes to a memory location in the second contiguous memory ~~space~~ section and ~~another~~ a second thread reads from another memory location in the second contiguous memory ~~space~~ section.

Claim 16 (Currently Amended): The computer program product of claim 15, wherein the ~~other~~ second thread reads ~~the other~~ from said another memory location ~~in the second memory space~~ after determining a read-after-write hazard does not exist for ~~the other~~ said another memory location ~~in the second memory space~~.

Claim 17 (Currently Amended): The computer program product of claim 14, further comprising:

instructions for allocating ~~additional~~ memory spaces in the additional contiguous memory ~~resource~~ sections to additional data buffers, each data buffer being accessible by ~~each thread in~~ any one of the plurality of threads.

Claim 18 (Currently Amended): The computer program product of claim 17, wherein [[the]] each data buffer is associated with a unique buffer identifier ~~and the additional data buffers are each associated with unique buffer identifiers~~.

Claim 19 (Currently Amended): A computing system comprising:

a memory resource;

a graphics processor coupled to the memory resource for executing one or more graphics program modules;

a central processing unit (CPU) coupled to the memory resource and the

graphics processor, wherein one of the CPU [[or]] and the graphics processor[[:]]

~~determines a first set of threads from a plurality of threads simultaneously executable in the graphics processor;~~

~~allocates a memory space to each thread in the first set of threads to respectively reserve the memory space; and~~

~~allocates an additional memory space accessible by each thread in the first set of threads to one or more data buffers to respectively reserve the additional memory space~~

is programmed to: (i) determine a set of threads, each of a same type, from a plurality of threads executable on a graphics processor; (ii) allocate memory spaces in a first contiguous memory section to the threads in said set of threads, said memory spaces in the first contiguous memory section being reserved for use by the threads in said set of threads; and (iii) allocate memory spaces in a second contiguous memory section to a data buffer, said memory spaces in the second contiguous memory section being accessible by any one of the plurality of threads.

Claim 20 (Currently Amended): The computing system of claim 19, further comprising:

~~an address unit coupled to the graphics processor and the CPU, wherein the address unit:~~

~~receives an access command from a thread in the first set of threads to access the memory space; and~~

~~determines if a read-after-write hazard exists prior to accessing the memory space~~

an address unit coupled to the graphics processor and the CPU, wherein the address unit is programmed to receive an access command from a thread in said set of threads to access one of the memory spaces in the first contiguous memory section and determine if a read-after-write hazard exists prior to accessing said one of the memory spaces in the first contiguous memory section.

Claim 21 (Original): The computing system of claim 20, wherein the address unit

uses an operation command and address request information to determine if a read-after-write hazard exists.

Claim 22 (Original): The computing system of claim 20, wherein the address unit uses a thread identification number and a memory location offset to determine if a read-after-write hazard exists.

Claim 23 (Currently Amended): The computing system of claim 19, further comprising:

~~an address unit coupled to the graphics processor and the CPU, wherein the address unit:~~

~~receives an access command from a thread in the first set of threads to access the additional memory space; and~~

~~determines if a read-after-write hazard exists prior to accessing the additional memory space~~

an address unit coupled to the graphics processor and the CPU, wherein the address unit is programmed to receive an access command from a thread in said set of threads to access one of the memory spaces in the second contiguous memory section, and determine if a read-after-write hazard exists prior to accessing said one of the memory spaces in the second contiguous memory section.

Claim 24 (Currently Amended): The computing system of claim [[19]] 23, wherein [[each]] the data buffer ~~in the additional memory space~~ is associated with a unique buffer identifier.

Claim 25 (Currently Amended): The computing system of claim 24, wherein the address unit uses the buffer identifier and ~~sample~~ position coordinates associated with a sample to determine if a read-after-write hazard exists.